BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 57-176456
(43)Date of publication of application : 29.10.1982

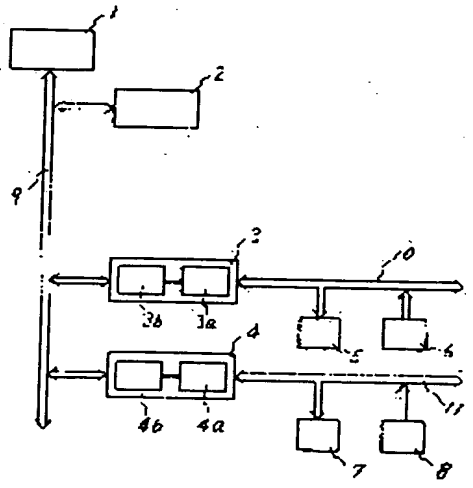
(51)Int.Cl. G06F 9/24

(21)Application number : 56-060965
(22)Date of filing : 22.04.1981

(71)Applicant : FANUC LTD
(72)Inventor : KURAKAKE MITSUO

(54) DATA PROCESSING SYSTEM

(57)Abstract:
PURPOSE: To make the change of a program easy, by transferring a control program from an ROM to an RAM of each microprocessor, and eliminating the need for the ROM per a control program of each microprocessor.
CONSTITUTION: A loading unit 2 is started with a power supply applied, the content of an ROM1 is read out and a required control program is stored to RAMs 3b and 4b of microprocessors 3 and 4 via a data bus 9. The loading unit 2 gives a start signal to the microprocessors 3 and 4 after the end of transfer, the microprocessors 3 and 4 respond it and start the operation according to the control program of the RAMs 3b and 4b. On the other hand, since an instruction is given from a main processor via the data bus 9, the microprocessors 3 and 4 control variables 5 and 7 via data buses 10 and 11.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

⑲ 日本国特許庁 (JP)　　⑪ 特許出願公開

⑫ 公開特許公報 (A)　　昭57—176456

⑤1Int. Cl.³	識別記号	庁内整理番号	⑬公開 昭和57年(1982)10月29日
G 06 F 9/24		8120—5B	

発明の数 1
審査請求 未請求

(全 3 頁)

⑤4データ処理方式

⑦1出 願 人 富士通フアナツク株式会社
日野市旭が丘3丁目5番地1

⑦2発 明 者 鞍掛三津雄
日野市旭が丘3丁目5番地1富士通フアナツク株式会社内

⑦4代 理 人 弁理士 辻實 外1名

②1特 願 昭56—60965
②2出 願 昭56(1981)4月22日

明 細 書

1. 発明の名称

データ処理方式

2. 特許請求の範囲

(1) ランダムアクセスメモリを内蔵したマイクロプロセッサと、該マイクロプロセッサの制御プログラムを収容した不揮発性メモリと、該不揮発性メモリの内容を該マイクロプロセッサに転送するローデイングユニットと、これらを接続するデータバスとを有し、該不揮発性メモリに収容された制御プログラムを該ローデイングユニットにより該マイクロプロセッサのランダムアクセスメモリに転送することを特徴とするデータ処理方式。

(2) 前記データバスに更に前記マイクロプロセッサを制御するメインプロセッサを接続することを特徴とする特許請求の範囲第(1)項記載のデータ処理方式。

(3) 前記マイクロプロセッサが前記データバスに複数接続されることを特徴とする特許請求の範囲第(1)項又は第(2)項記載のデータ処理方式。

(4) 前記マイクロプロセッサに制御対象となる入出力ユニットが別のデータバスを介し接続されることを特徴とする特許請求の範囲第(1)項又は第(2)項又は第(3)項記載のデータ処理方式。

(5) 前記ローデイングユニットはメモリとマイクロプロセッサで構成されることを特徴とする特許請求の範囲第(1)項又は第(2)項又は第(3)項又は第(4)項記載のデータ処理方式。

(6) 前記制御対象がモータであることを特徴とする特許請求の範囲第(4)項記載のデータ処理方式。

3. 発明の詳細な説明

本発明は、容易に自己の制御プログラムを変更しうるデータ処理方式に関し、特にメモリを内蔵するマイクロプロセッサに好適なデータ処理方式に関する。

近年マイクロプロセッサはその集積度が向上し、又演算速度の向上に伴い各種装置の制御用に盛んに利用されている。かゝる、制御用マイクロプロセッサとしては、制御プログラムを収容しうるメモリを内蔵した1チップ化したマイクロプロセッ

サが便利である。ところで、この様な制御プログラムを内蔵するメモリとしては、電源の供給停止時にも記憶内容を消失しないリードオンリーメモリ（以下ＲＯＭと称す）が用いられているが、制御プログラムの変更が容易でない欠点がある。即ち、１チップマイクロプロセッサに内蔵されるＲＯＭは、殆んどマスクロム（mask ＲＯＭ）であり、プログラムの変更が容易でない。尚、イレーザブルROM（Erasable ＲＯＭ）を内蔵するものもあるが、mask ＲＯＭに比べてＬＳＩのチップが大きくなるため、価格、供給、信頼性に問題がある。

以上の点を数値制御システムにおけるサーボモータ制御について具体的に説明する。さて、数値制御システムにおけるサーボモータの制御にマイクロプロセッサを用いる場合には、対象のモータ毎にあるいは、制御方式毎に多数の制御プログラムが用意されている。このためこの中からモータ制御に応じた所定の制御プログラムを選択し、該制御プログラムに基いてモータを制御する必要がある。このように所定の制御プログラムを選択し

て正しくモータを制御するためにはメモリとして外付けのイレーザブルROM（ＥＲＯＭ）を用い、該ＥＲＯＭにモータ或いはモータ制御に応じた制御プログラムを書込むことが考えられるが、１チップ化したプロセッサ以外にＲＯＭが必要となるので部品点数が増加し得策でない。又、１つのROMに複数の制御プログラムを収容することも考えられるが、これらの制御プログラムを全て収容するには、ROMの容量が大きくなり、コスト、実装スペースから不利である。

従つて、本発明は、マイクロプロセッサ内部に記憶される制御プログラムを容易に変更しうる新規なデータ処理方式を提供することを目的とするものである。

以下、本発明を実施例により詳細に説明する。

図面は本発明の一実施例ブロック図を示し、図中、１は制御プログラムを格納する不揮発性メモリで、例えばバブルメモリー、ＲＯＭで構成される。２は不揮発性メモリ１の内容を読出し転送するローディングユニットで、ROM又はランダムアクセ

スメモリ（以下RAMと称す）を内蔵するマイクロプロセッサで構成される。３及び４はマイクロプロセッサで、各々プロセッサ本体３ａ及び４ａと、プロセッサ３ａ，４ａの制御プログラムを格納するためのRAM３ｂ及び４ｂとで構成される。５及び７はマイクロプロセッサ３，４に制御される出力ユニットであり、この例ではモータを示す。６及び８は入力ユニットであり、この例では、マイクロプロセッサ３，４にモータの状態たとえば回転速度を検知して出力する検知器を示す。９は不揮発性メモリ１、ローディングユニット２、マイクロプロセッサ３，４を相互に接続するメインデータバスであり、数値制御のメインプロセッサにも接続されている。尚、メインプロセッサより移動指令、指令速度などがデータバスを介してマイクロプロセッサ３，４に入力される。１０，１１はマイクロプロセッサ３，４と、出力ユニット５，７及び入力ユニット６，８とを相互に接続するデータバスである。

次にこれらの動作について説明する。

不揮発性メモリ１には、各種モータの制御のた

めの各種の制御プログラムが格納されている。又、マイクロプロセッサ３，４の各々は数値制御における各制御軸毎に用意されていると仮定する。

先づ、電源が投入されると、該電源の投入を検知してローディングユニット２が起動し、ローディングユニット２は自己の制御プログラムに従い不揮発性メモリ１の内容を読出す。そして、予じめ各マイクロプロセッサ３，４の必要とする制御プログラムがわかつているので、ローディングユニット２は各マイクロプロセッサ３，４のRAM３ｂ，４ｂにデータバス９を介し必要とする制御プログラムを転送し、制御プログラムをRAM３ｂ，４ｂに格納せしめる。

ローディングユニット２は更に転送終了後に各マイクロプロセッサ３，４にスタート信号をデータバス９を介して送り、マイクロプロセッサ３，４は、これに応答し、RAM３ｂ，４ｂの制御プログラムに従い動作を開始する。一方、図示しない前述のメインプロセッサからデータバス９を介して速度指令、移動数値指令が与えられるから、各マイ

クロプロセッサ3，4はデータバス10，11を介し制御対象であるモータ（出力ユニット）5及び7を制御することになる。

尚、数値制御システムでは、もともと各種パラメータや加工データの収容のために不揮発性メモリを備えているから、前述の不揮発性メモリ1を特別設けることなく、このメモリの一部を利用してもよい。

以上の説明では、数値制御システムを例にして説明した、これに限ることなく、他の制御システムにも利用することができる。

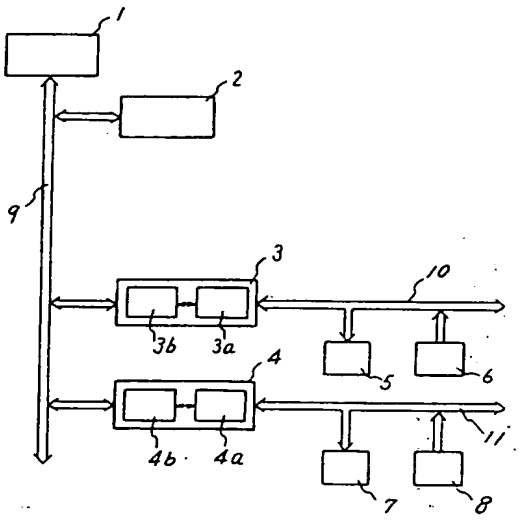
以上説明した様、本発明によれば、制御プログラムを格納した不揮発性メモリから各マイクロプロセッサのランダムアクセスメモリに制御プログラムを転送する様構成したので、各マイクロプロセッサに制御プログラム毎にROMを持つ必要はなく、制御プログラムの変更が容易に達成出来、特に複雑な制御が要求される数値制御システムに極めて有用である。

4. 図面の簡単な説明

図面は本発明の一実施例ブロック図を示す。

図中、1…不揮発性メモリ、2…ローディングユニット、3，4…マイクロプロセッサ、3a，4a…プロセッサ本体、3b，4b…ランダムアクセスメモリ、9…データバス。

特許出願人　富士通ファナック株式会社
代理人　弁理士　辻　實
外1名



(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 077 404**
A1

(12) # EUROPEAN PATENT APPLICATION

published in accordance with Art. 158(3) EPC

(21) Application number: 82901162.6

(22) Date of filing: 22.04.82

Date of the international application taken as a basis:

(86) International application number:
PCT/JP82/00138

(87) International publication number:
WO82/03708 (28.10.82 82/26)

(51) Int. Cl.³: G 06 F 3/00
G 06 F 13/00, G 06 F 9/06
G 05 B 19/02

(30) Priority: 22.04.81 JP 60965/81

(43) Date of publication of application:
27.04.83 Bulletin 83/17

(84) Designated Contracting States:
CH DE FR GB LI

(71) Applicant: Fanuc Ltd
5-1, Asahigaoka, 3-chome
Hino-shi, Tokyo 191(JP)

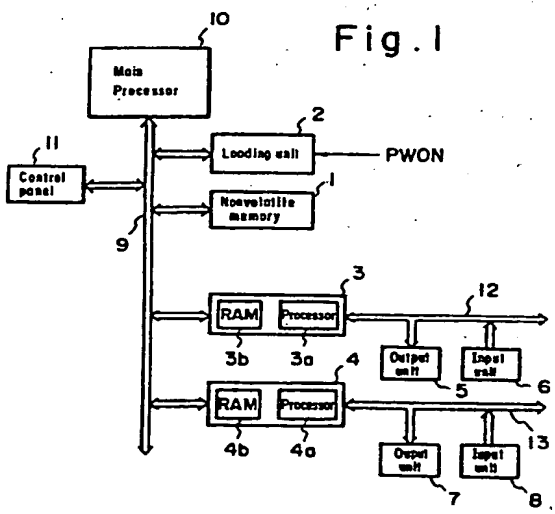
(72) Inventor: KURAKAKE, Mitsuo
Izumi-Haitsu 103 3-3-10, Tamadaira
Hino-shi Tokyo 191(JP)

(74) Representative: Billington, Lawrence Emlyn et al,
HASELTINE LAKE & CO Hazlitt House 28 Southampton
Buildings Chancery Lane
London WC2A 1AT(GB)

(54) **DATA PROCESSING SYSTEM.**

(57) Microprocessors (3, 4) containing random access memories (RAM) (3b, 4b), a non-volatile memory (1) containing the control program of the microprocessors, and a loading unit (2) for transferring the content of the non-volatile memory to the microprocessors are connected via a data bus (9). Since the control program is transferred from the nonvolatile memory to the random access memory in the microprocessors in accordance with the relative relationship between the control program specified on the control panel (11) and the microprocessors when power is applied, the execution control program is facilitated.

Fig. 1



EP 0 077 404 A1

0077404

DESCRIPTION

DATA PROCESSING SYSTEM

Technical Field:

The present invention relates to a data processing system which can readily change a control program of its own, and more particularly to a data processing system which is well-suited for use in a microprocessor having a built-in memory.

Background Art:

In recent year, microprocessors have been extensively utilized for controlling various apparatuses with enhancement in the density of integration and enhancement in the operating speed. As such a controlling microprocessor, a microprocessor in the form of a single chip having a built-in memory capable of receiving a control program is convenient. In this regard, a read-only memory (hereinbelow, termed "ROM"), the stored content of which is not erased even when the supply of power is terminated, is used as the aforementioned memory for storing the control program but is disadvantageous in that it is not easy to change the control program. Mor specifically, most ROMs built in 1-chip microprocessors are mask ROMs, which cannot readily change programs. Although erasable ROMs are built in some 1-chip microprocessors, they have problems in price, supply and reliability because of larger LSI chips than in the mask ROMs.

The above points will be concretely described with regard to a servomotor control in a numerical control system. When applying a microprocessor to the control of a servomotor in a numerical control system, a large number of control programs are prepared for each motor or each control system which is to be controlled. Therefore, a predetermined control program suited to the motor control must be selected from among the control programs, so as to control the motor on the basis of the selected control program. To the end of selecting the predetermined control program and properly controlling the motor in this manner, it has been considered to employ an erasable ROM (EROM) mounted externally of the microprocessor, as the microprocessor memory, and to write the control program suited to the motor or the motor control, into the EROM. Since, however, the measure of employing the external EROM necessitates the ROM besides the processor fabricated in the form of a single chip, it increases the number of components and is not recommendable. It has also been considered to accommodate a plurality of control programs in a single ROM. However, the ROM requires a large capacity in order to receive all the control programs. This is disadvantageous from the standpoints of cost and installation space.

Accordingly, the present invention has for its object

to provide a novel data processing system which can readily change a control program stored within a microprocessor.

Disclosure of the Invention:

Disclosed in the present invention is a data processing system comprising a microprocessor having an internal random access memory, a nonvolatile memory in which control programs of the microprocessor are stored, a loading unit which transmits the content of the nonvolatile memory to the microprocessor, and a data bus which connects them, whereby the control program stored in the nonvolatile memory is transmitted to the random access memory of the microprocessor by the loading unit, so as to process data in accordance with this control program. This data processing system is so constructed as to transmit the control program from the nonvolatile memory storing the control programs, to the random access memory of each microprocessor. Therefore, each microprocessor need not be equipped with ROMs for the various control programs and the change in control programs can be achieved with ease. In particular, the system is very useful for a numerical control system in which complicated control is required.

Brief Description of the Drawings:

Figure 1 is a block diagram of an embodiment of the present invention.

Best Mode for Carrying out the Invention:

The present invention will now be described in detail in connection with an embodiment.

Figure 1 shows a block diagram of one embodiment of the present invention. In the figure, numeral 1 designates a nonvolatile memory which stores control programs and which is constructed of, for example, a bubble memory or a ROM. Numeral 2 designates a loading unit which reads out and transmits the content of the nonvolatile memory 1, and which is constructed of a microprocessor having a built-in ROM or random access memory (hereinbelow, termed "RAM"). Microprocessors 3 and 4 are respectively constructed of processors proper 3a and 4a, and RAMs 3b and 4b for storing the control programs of the processors 3a and 4a. Numerals 5 and 7 indicate output units which are controlled by the microprocessors 3, 4, and which are motors in this example. Numerals 6 and 8 indicate input units, which are, in this example, detectors that detect the states of the motors, e.g., the rotating speeds thereof and deliver them to the microprocessors 3, 4. Shown at numeral 9 is a main data bus which connects the nonvolatile memory 1, loading unit 2 and microprocessors 3, 4 to one another, and which is also connected to a main processor 10, a control panel 11, etc. for the numerical control. Move commands, commanded speeds, etc. are

entered from the main processor 10 to the microprocessors 3, 4 through the data bus. Data buses 12, 13 interconnect the microprocessors 3, 4, output units 5, 7 and input units 6, 8.

Next, the operations of these constituents will be explained.

In the nonvolatile memory 1, various control programs for controlling the respective motors are stored with identifier codes (for example, names) assigned thereto. In addition, it is assumed that the respective microprocessors 3 and 4 are prepared for the respective controllable axes in the numerical control.

When power from a power supply is introduced (a power "on" signal PWON goes to logical "1"), the loading unit 2 starts upon sensing the introduction power and reads out the content of the nonvolatile memory 1 in accordance with a control program of its own stored in the built-in ROM. The corresponding relationships between the respective microprocessors 3, 4 and the identification numbers, e.g., control program names of the control programs required for these microprocessors are set with the control panel 11 in advance. Accordingly, the loading unit 2 transmits the required control programs to the RAMs 3b, 4b of the respective microprocessors 3, 4 through the data bus 9 while referring to the corresponding relationships and

stores them in the RAMs 3b, 4b.

The loading unit 2 further sends start signals to the respective microprocessors 3, 4 through the data bus 9 after the end of the above transmission. In response to the signals, the microprocessors 3, 4 start operating in accordance with the control programs of the RAMs 3b, 4b. On the other hand, speed commands and movement value commands are given from the aforementioned main processor through the data bus 9, so that the respective microprocessors 3 and 4 control the motors (output units) 5 and 7 through the data buses 12 and 13.

A numerical control system is originally equipped with a nonvolatile memory in order to store various parameters and machining data. Therefore, a part of this memory can be utilized without specially providing the nonvolatile memory 1 stated before. In addition, the corresponding relationships between the control programs and the microprocessors must be easily settable and changeable. However, once they have been set, they are hardly ever altered. Switches are therefore disposed inside the control panel or the like so as to establish semifixed relationships, in order that the corresponding relationships may be set by means of only the switches. This measure prevents changes in the corresponding relationships and a resulting malfunction as may be caused by

accidental operation attributed to the fact that switches protrude from the outside of the apparatus.

Although a numerical control system has been exemplified in the above description, the invention is not restricted thereto but is also utilizable for other control systems.

Industrial Applicability:

As set forth above, according to the present invention, a data processing system is so constructed as to transmit a control program from a nonvolatile memory storing control programs, to the random access memory of each microprocessor. Therefore, each microprocessor need not be equiped with ROMs for the respective control programs, and a change in control programs can be achieved with ease. In particular, the system is very useful for a numerical control system in which complicated control is required.

WHAT IS CLAIMED IS:

1. A data processing system characterized by comprising a microprocessor having an internal random access memory, a nonvolatile memory in which control programs of said microprocessor are stored, a loading unit which transmits the content of said nonvolatile memory to said microprocessor, and a data bus which connects them, whereby the control program stored in said nonvolatile memory is transmitted to said random access memory of said microprocessor by said loading unit.

2. A data processing system as defined in Claim 1, characterized in that a main processor for controlling said microprocessor is further ocnnected to said data bus.

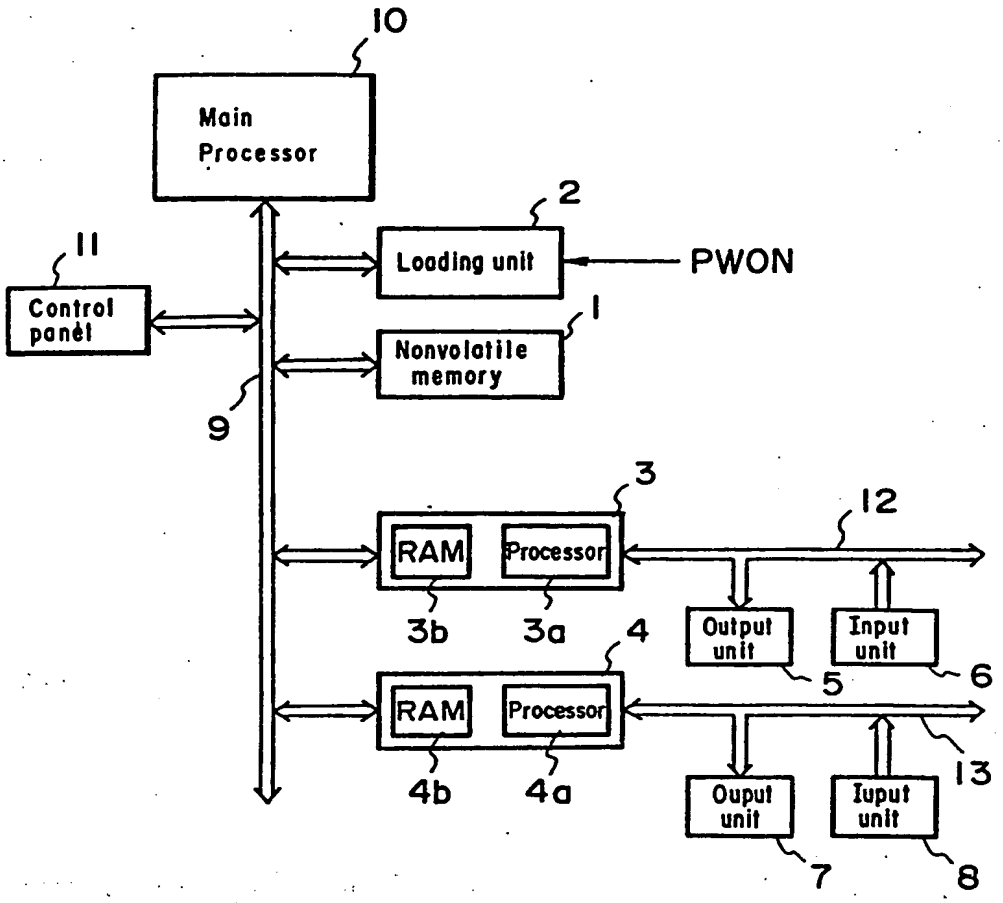
3. A data processing system as defined in Claim 1 or Claim 2, characterized in that a plurality of such microprocessors are connected to said data bus.

4. A data processing system as defined in Claim 1, Claim 2 or Claim 3, characterized in that an input/output unit to be controlled is connected to said microprocessor through another data bus.

5. A data processing system as defined in Claim 1, Claim 2, Claim 3 or Claim 4, characterized in that said loading unit is constructed of a memory and a microprocessor.

6. A data processing system as defined in Claim 4, characterized in that said unit to be controlled is a motor.

Fig. 1


10
Main Processor
2
Loading unit
PWON
11
Control panel
1
Nonvolatile memory
9
3
12
RAM
Processor
3b
3a
Output unit
Input unit
5
6
4
RAM
Processor
4b
4a
13
Ouput unit
Iuput unit
7
8

INTERNATIONAL SEARCH REPORT 0077404

International Application No. PCT/JP 82/00138

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)

According to International Patent Classification (IPC) or to both National Classification and IPC

Int Cl[3] G06F 3/00, G06F 13/00, G06F 9/06, G05B 19/02

II. FIELDS SEARCHED

Minimum Documentation Searched

Classification System	Classification Symbols
IPC	G06F 3/00, G06F 13/00, G06F 9/06 G05B 19/02

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched

Kokai Jitsuyo Shinkan Koho 1971-1781

III. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
X	JP, A, 50-109635 (Hitachi, Ltd.) 28. August, 1975 (28.08.75)	1-6
X	JP, A, 54-114136 (Hitachi, Ltd.) 6. September, 1979 (06.09.79)	1-6
X	JP, A, 55-41553 (Fujitsu Ltd.) 24. March, 1980 (24.03.80)	1-6
A	JP, A, 53-63836 (Nippon Telegraph & Telephone Public Corp.) 7. June, 1978 (07.06.78)	1-6

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
July 20, 1982 (20.07.82)	July 26, 1982 (26.07.82)
International Searching Authority	**Signature of Authorized Officer**
Japanese Patent Office	